

We claim:

1. A method for cycling through addresses of a memory device, comprising:
generating for each address a respective bit pattern comprised of a predetermined
number of bits; and

5 cycling through the respective bit pattern for each of the addresses with a transition
of less than the predetermined number of bits for sequencing to each subsequent address.

2. The method of claim 1, further comprising:
cycling through the respective bit pattern for each of the addresses in a gray code
10 sequence.

3. The method of claim 2, wherein the memory device is a flash memory device.

4. The method of claim 3, further comprising:
15 eliminating charge gain failure of the flash memory device.

5. The method of claim 2, further comprising:
generating a respective binary bit pattern for each of the addresses;
converting the respective binary bit pattern to a respective gray code bit pattern for
20 each of the addresses; and
using the respective gray code bit pattern by address decoders for accessing the
memory device.

6. The method of claim 2, further comprising:
25 heating the memory device such that the step of cycling through the respective bit
pattern for each of the addresses is performed during a test for HTOL (high temperature
operating life) of the memory device.

7. The method of claim 1, further comprising:
30 cycling through the respective bit pattern for each of the addresses with a transition
of a fixed number of bits for sequencing to each subsequent address.

8. The method of claim 1, wherein the memory device is a flash memory device.

9. The method of claim 8, further comprising:

eliminating charge gain failure of the flash memory device.

10. The method of claim 1, further comprising:

heating the memory device such that the step of cycling through the respective bit pattern for each of the addresses is performed during a test for HTOL (high temperature operating life) of the memory device.

11. A system for cycling through addresses of a memory device, comprising:

an address generator for generating for each address a respective bit pattern comprised of a predetermined number of bits; and

means for cycling through the respective bit pattern for each of the addresses with a transition of less than the predetermined number of bits for sequencing to each subsequent address.

12. The system of claim 11, further comprising:

a gray code converter for cycling through the respective bit pattern for each of the addresses in a gray code sequence.

13. The system of claim 12, wherein the memory device is a flash memory device.

14. The system of claim 13, wherein charge gain failure of the flash memory device is eliminated.

15. The system of claim 12, wherein the address generator generates a respective binary bit pattern for each of the addresses, and wherein the gray code converter converts the respective binary bit pattern to a respective gray code bit pattern for each of the addresses, and wherein the system further comprises:

address decoders for decoding the respective gray code bit pattern for accessing the memory device.

16. The system of claim 12, further comprising:

5 a heater for heating the memory device such that cycling through the respective bit pattern for each of the addresses is performed during a test for HTOL (high temperature operating life) of the memory device.

17. The system of claim 11, further comprising:

10 mean for cycling through the respective bit pattern for each of the addresses with a transition of a fixed number of bits for sequencing to each subsequent address.

18. The system of claim 11, wherein the memory device is a flash memory device.

15 19. The system of claim 18, wherein charge gain failure of the flash memory device is eliminated.

20. The system of claim 11, further comprising:

20 a heater for heating the memory device such that cycling through the respective bit pattern for each of the addresses is performed during a test for HTOL (high temperature operating life) of the memory device.